Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **1 OUT**
2. **1 IN-**
3. **1 IN+**
4. **VDD+**
5. **2 IN+**
6. **2 IN-**
7. **2 OUT**
8. **N. ½ SHDN**
9. **N. ¾ SHDN**
10. **3 OUT**
11. **3 IN-**
12. **3 IN+**
13. **GND**
14. **4 IN+**
15. **4 IN-**
16. **4OUT**

**.045”**

**.080”**

**1 16**

**2**

**3**

**4**

**5**

**6**

**7**

**8 9**

**15**

**14**

**13**

**12**

**11**

**10**

**MASK**

**REF**

**TLV2375**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential: Floating**

**Mask Ref: TLV2375**

**APPROVED BY: DK DIE SIZE .045” X .080” DATE: 3/27/23**

**MFG: TEXAS INSTRUMENTS THICKNESS .012” P/N: TLV2375**

**DG 10.1.2**

#### Rev B, 7/19/02